Processor Tiles

- Partition all major structures into banks, distribute, and interconnect
- Execution Tile (E)
  - 64-entry Instruction Queue bank
  - Single-issue execute pipeline
- Register Tile (R)
  - 32-entry Register bank (per thread)
- Data Tile (D)
  - 8KB Data Cache bank
  - LSQ and MHU banks
- Instruction Tile (I)
  - 16KB Instruction Cache bank
- Global Control Tile (G)
  - Tracks up to 8 blocks of insts
  - Branch prediction & resolution logic