Faster Virtualization Performance

- Nested Paging (NP)
  - Guest and Host page tables both exist in memory
    The processor walks both guest and host page tables
  - Nested walk can have up to 24 memory accesses!
    Hardware caching accelerates the walk
  - "Wire-to-wire" translations are cached in TLBs
  - NP eliminates Hypervisor cycles spent managing shadow pages
    As much as 75% of Hypervisor time

- Barcelona also reduces world-switch time by 25%
  - World-switch time : round-trip to the Hypervisor and back