Delivering more DRAM bandwidth

- Independent DRAM controllers
- Optimized DRAM paging
- Re-architect NB for higher BW
- Write bursting
- **DRAM prefetcher**
  - **Track positive and negative, unit and non-unit strides**
  - **Dedicated buffer for prefetched data**
  - **Aggressively fill idle DRAM cycles**
- Core prefetchers