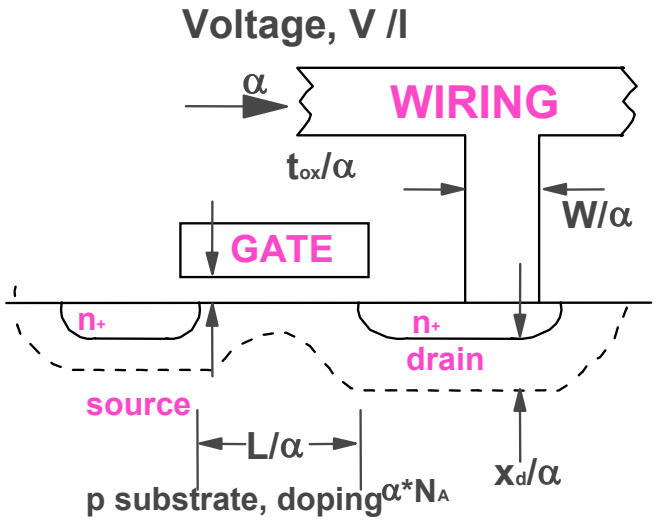
Classical CMOS Scaling



SCALING:

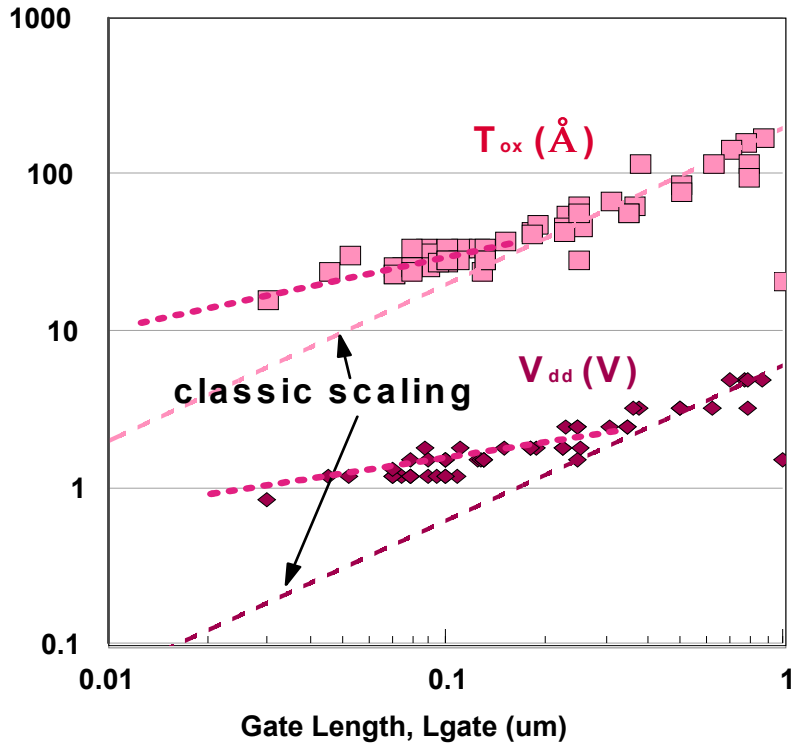
Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

RESULTS:

Higher Density:	$\sim a^2$
Higher Speed:	$\sim a$
Power/ckt:	$\sim 1/a^2$

Power Density:~Constant

Is it Really Dead?



Why deviate from "ideal" scaling

- unacceptable gate leakage/reliability
- additional performance at higher voltage

What is consequence of this deviation?

- **a dramatic rise in power density**