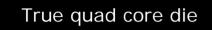
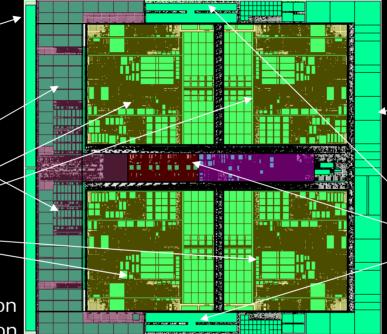
A Closer Look at AMD's Next Generation Server and Desktop Architecture



- Expandable shared L3 cache
- IPC enhanced CPU cores
- 32B instruction fetch
- Enhanced branch prediction
- Out-of-order load execution
- Up to 4 DP FLOPS/cycle
- Dual 128-bit SSE dataflow
- Dual 128-bit loads per cycle
- Bit Manipulation extensions (LZCNT/POPCNT)
- SSE extensions (EXTRQ/INSERTQ, MOVNTSD/MOVNTSS)



Optimized for 65nm SOI and beyond

- Enhanced Direct
- Connect Architecture
- _ and Northbridge
 - HT-3 links (Up to 5.2GT/sec)
 - Enhanced crossbar
 - DDR2 with migration path to DDR3
 - FBDIMM when appropriate
 - Enhanced power management
 - Enhanced RAS