AMD's Silicon-Level Innovation Priorities through 2008

CPU Silicon

Instruction Set Architecture

- Partitioned AMD PowerNow! technology
- FPU extensions
- Pacifica virtualization, Presidio security

Microarchitecture

- HyperTransport™ technology 3.0 and 4.0
- Multi-core architecture
- Scalable SMP architecture
- On-chip coprocessors

Process Technologies

- 65nm technology generation
- 3rd generation strained silicon
- 4th generation low-k stack
- 45nm technology generation

- Making the best, better: Direct Connect Architecture will continue to improve
- Selectively license coherent HyperTransport™ technology
- Ensuring compatibility while adding functionality
- Successful joint development agreement with IBM has been extended