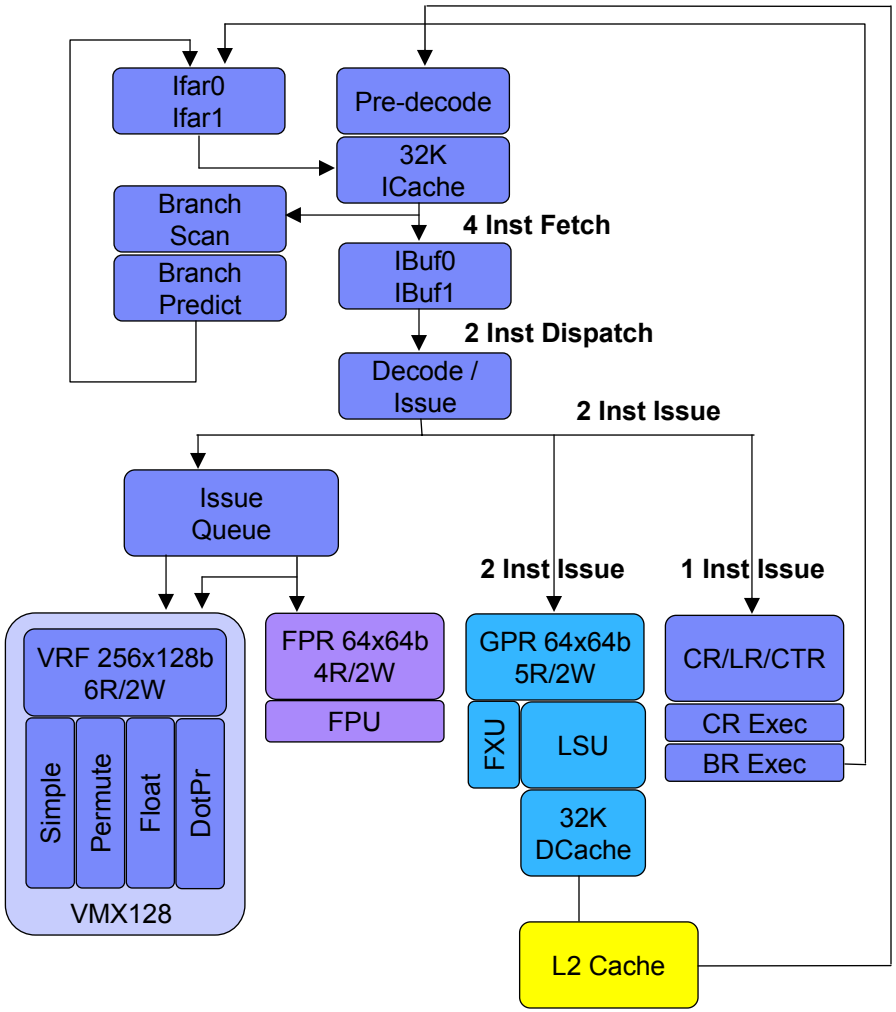
64b IBM PowerPC® -Architecture Core



- Highest Freq Power PC® ISA Core: 11 FO4
- Extensive Clock Gating for power efficiency
  - Pipelines shutdown until instruction active
- Instruction Unit
  - Multithreading – 2 simultaneous threads
  - ICache: 32KByte, 2 way, 128B line
  - 64 entry, 2 way, 1st level translation (ERAT)
  - 4Kx2 BHT per thread w/ Global Gshare
  - Two instruction In-Order Issue
  - Delayed execution to cover load use penalty
- Fixed Point and Load/Store execution
  - 2 FXU units – Simple / Complex
  - 2 cycle ALU op latency
  - 2 cycle fixed pt Ld latency - delayed execution
  - DCache
    - 32KByte, 4 way, 128 B line, store-thru
    - Non-blocking (hit under miss)
  - 64 entry, 2 way, 1st level translation (ERAT)
  - 1K, 4 way, 2nd level translation (TLB)
  - 8 entry MissQ, 16 entry StoreQ